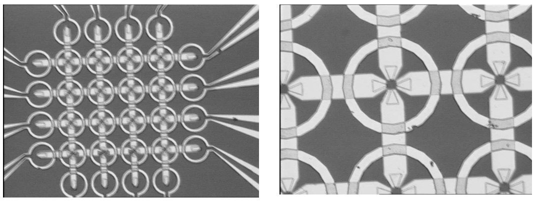
GUIDED MAGNETIC FLUX TRAPPING FOR QUANTUM INFORMATION PROCESSING

CHRISTOPH KERNER, WIM MAGNUS AND WIM SCHOENMAKER
IMEC, Kapeldreef 75, 3001 Leuven, Belgium.
E-mail: kernerc@imec.be, magnus@imec.be, schoen@imec.be

CHRIS VAN HAESENDONCK
Solid-State Physics Dept., University of Leuven, Celestijnenlaan 200D, 3001 Leuven, Belgium.
E-mail: chris.vanhaesendonck@fys.kuleuven.ac.be

We propose controlled magnetic flux guiding and trapping in micron-sized, superconducting metal rings for quantum information processing [1]. A ring-array realized through circuit design and silicon processing technology could set the necessary physical and quantum mechanical conditions needed for a solid-state quantum bit (qbit) register, the basis of a quantum computer. Theoretical aspects include simulating the described device [2] but do not take quantum algorithms and their executions into account. The understanding and possible *beneficial* usage of quantum effects represents a crucial factor in tomorrow's semiconductor industry, as we're trying to keep up with Moore's law, downscaling chip-component sizes to make chips faster. Furthermore, quantum information processing and quantum computing are very modern topics on their own, pointing to new ways of computing and are impacting on conventional layouts and operation schemes.

The idea of using quantum mechanical principles for operating computers in a possibly beneficial manner dates back to the 1980's and was eventually supported by quantum algorithms such as Grover's database search algorithm [3] or Shor's factoring algorithm in the mid 1990's. Demonstrating substantial computational speed-up with respect to the today's classical computing, these algorithms spurred on experimentalists to realize first quantum computations soon after, where today's qbit layouts range from ion traps, *QED, NMR*- and superconducting devices [4] to artificial atoms and more. The underlying principle is to define a two-level quantum system (qbit), representing the two basic states 0 and 1 (using spins, magnetic moments, persistent currents etc.) and to be able to manipulate these or switch between them via external signals. Any two-level quantum system may be found in a linear combination of the basis states (superposition principle), moreover, a full qbit register can be put into an entangled state of superposition, coherently connecting all qbits until an answer is read out and decoherence destroys the entanglement. Thus, parallel computing becomes possible, with system space growing exponentially with the number of added qbits. Future quantum computer hardware will most likely rely on simple, cheap solid-state layouts, easily scalable and reproducible. Keeping this in mind, we set up a qbit layout, to be realized within IMEC silicon processing technology. We propose to use an array of micron-sized aluminium rings (computing elements), surrounded by semi-closed rings connected to bonding pads for access (input/output). Applying alternating current signals to an input port induces a magnetic field which itself can induce a current in a nearby, free ring, relying on Faraday's induction principle. In order to minimize system loss and prohibit magnetic field lines from spreading out in space we use ferromagnetic core-elements (75% nickel, 25% iron), inter-connecting the rings (without galvanic contact). The core-confined field lines are thus guided through the ring array, exploiting a transformer-like effect. As the system is cooled down below 1.23 K, the free aluminium rings become superconducting, trapping magnetic flux (in multiples of the flux quantum), giving rise to persistent currents. Thus, the trapping of zero or one flux quantum can be selected as the basic states 0 and 1 and the arising persistent currents measured. In order to be able to switch between 0 and 1 or to trap an extra flux quantum in a ring, the superconducting state has to be momentarily destroyed (switching to the normal conducting state). This can be achieved by reaching the critical current value inside a superconducting ring. Experimentally achieved quantum effects should leave measurable signatures in the output. A device design has been made and corresponding lithography masks manufactured, dividing the layout into four masks levels, 1. horizontal core-part, 2. rings/bonding pads, 3. vertical core-part, 4. bonding pad passivation windows. Five process cycles are required to transfer the design onto silicon wafers following the pattern: Wafer clean/dehydration bake, resist spin/hard bake, mask-level alignment and UV exposure (pattern definition), development/inspection, metallization and lift-off (pattern transfer). The gaps between the metal layers are provided by an insulator (CVD-deposited silicon-oxide) and insulator trenches are (dry-)etched, using a reactive ion beam (RIE). Measurements are being conducted on a MFM apparatus with future extension to SQUID measurements. Using our results from previous test structures, first full devices have just been manufactured and (unpublished) measurement data should be available by the start for the workshop.



Figures (ring-array)
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